AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1. (Currently Amended) A semiconductor memory device, comprising:

a non-volatile main storage memory including a plurality of physical blocks, each physical block ~~storage region consisting of~~ having a plurality of storage capacity units ~~which are~~ composed of a data region in a first storage capacity and a management region;

an address management information storage ~~part for storing~~ that stores address management information of said main storage memory and a block status of each physical block indicating whether data stored in the block is valid or not;

a non-volatile control memory ~~for storing~~ that stores a writing completion flag table which is provided to said ~~corresponding~~ main storage memory every second storage capacity [[unit]] smaller than said first storage capacity and consists of writing completion flags placed when data writing is completed to each of said second storage capacity; and

a ~~control part for performing~~ controller that performs read/write control for said main storage memory in accordance with a direction of data read/write from a host and for performing update control for said address management information storage part and said non-volatile control memory.

2. (Currently amended) The semiconductor memory device according to claim 1, wherein

said second storage capacity [[unit]] is a cluster size, and

said non-volatile control memory records the writing completion flag table ~~consisting of~~ by writing completion flags of at least one bit for every cluster size prescribed by a file system of the host.

3. (Currently amended) The semiconductor memory device according to claim 1, wherein

said second storage capacity [[unit]] is a sector size, and

said non-volatile control memory records the writing completion flag table ~~consisting of~~ by writing completion flags of at least one bit for every sector size prescribed by a file system of the host.

4. (Cancelled)

5. (Currently amended) The semiconductor memory device according to claim 1, wherein

said non-volatile control memory has a higher writing-rate than that of said non-volatile main storage memory.

6. (Currently amended) The semiconductor memory device according to claim 1, wherein

said ~~control part composes~~ controller includes a memory map of the writing completion flag table at initialization or factory shipment, based on a preliminarily stored second storage capacity unit.

7. (Currently amended) The semiconductor memory device according to claim 1, wherein

said ~~control part composes~~ controller includes a memory map of the writing completion flag table at initialization or factory shipment, based on a second storage capacity unit transferred from the host.

8. (Currently amended) The semiconductor memory device according to claim 1, wherein

said non-volatile main storage memory [[is]] comprises a multi-valued NAND flash memory.

9. (Currently amended) The semiconductor memory device according to claim 1, wherein

said address management information storage ~~part~~ includes [[:]] a physical region management table ~~for storing~~ that stores conditions for every storage capacity unit of said main storage memory; and an address conversion table ~~for converting~~ that converts an address designated by a file system of the host into an address of a storage capacity unit of said main storage memory.

10. (Currently amended) The semiconductor memory device according to claim 1, wherein

said control memory [[is]] comprises a ferroelectric random access memory (FeRAM).

11. (Currently amended) The semiconductor memory device according to claim 1, wherein

said control memory [[is]] comprises a magnetic random access memory (MRAM).

12. (Currently amended) The semiconductor memory device according to claim 1, wherein

said control memory [[is]] comprises an ovonic unified memory (OUM).

13. (Currently amended) The semiconductor memory device according to claim 1, wherein

said control memory [[is]] comprises a resistance RAM (RRAM).